Better Pictures Through Physics

The state of the art of CMOS image sensors.

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Over the last decade, CMOS image sensor technology has made huge progress. Not only has the imager's performance improved drastically, but there has also been great commercial success since the introduction of mobile phones with onboard cameras. Many scientists and marketing specialists predicted 15 years ago that CMOS image sensors were going to take over completely from charge coupled device (CCD) imagers, just as CCD imagers took over the imaging business from tubes in the mid-1980s [1].

Although CMOS technology has a strong position in imaging today, it has not obliterated the CCD business. The CMOS push has actually drastically increased the size of the overall imaging market because CMOS image sensors created new application areas that have boosted the performance and market for CCD imagers as well.

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Impact of CMOS Scaling on Image Sensors

It is common knowledge that scaling effects in CMOS technology allow the semiconductor industry to make smaller devices. This rule holds for CMOS imaging applications as well.

Figure 1 provides an overview of CMOS imager data published at the International Electron Devices Meeting (IEDM) and the International Solid-State Circuits Conference (ISSCC) over the last 15 years [2].

The blue line in Figure 1 illustrates the CMOS scaling effects over the years, as described by the ITRS road map [3]. The green line shows the technology node used to fabricate the reported CMOS image sensors, and the red line illustrates the pixel size of the same devices.

The following points should now be clear:

- CMOS image sensors use a technology node that lags behind the technology nodes of the ITRS. The reason for this is quite simple: Very advanced CMOS processes used to fabricate digital circuits are not imaging-friendly because of issues such as large leakage current, low light sensitivity, noise performance, and so on.

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- CMOS image sensor technology scales at almost the same pace as standard digital CMOS processes.
- Pixel dimension scales with the technology node used, and the ratio of pixel size over technology node is about a factor of 20.

Shrinking the pixel size for CMOS image sensors is a very important driver for the overall imaging business. It has a very large impact on various parameters of the complete camera system. For instance, if the pixel size or pitch of a CMOS image sensor is equal to p, then the scaling factors for various parameters, keeping the total pixel count unchanged, are as follows:

- pixel pitch: $\sim p$
- pixel area: $\sim p^2$
- chip area: $\sim p^2$
- chip cost: $\sim p^2$
- energy to read the sensor: $\sim p^2$
- lens volume: $\sim p^3$
- camera volume: $\sim p^3$
- camera weight: $\sim p^3$.

From this list it is clear that there is a very strong force driving the industry to shrink pixel size as much as possible. Unfortunately, making pixels smaller exerts a negative effect on their optical and electrical performance. The relation between pixel size and certain measures of camera performance is generally as follows:

- depth of field: $\sim p^{-1}$
- depth of focus: $\sim p^{-1}$
- signal-to-noise ratio: $\sim p^{-2}$
- dynamic range: $\sim p^{-2}$.

The effects of shrinking a pixel can be summarized as follows: as long as a camera stays in its packaging, smaller pixels have only advantages. Once the camera is switched on, however, smaller pixels bring only disadvantages.

The market for consumer applications is demanding smaller pixel sizes at the same time that progress in CMOS technology is offering the means to fabricate them. But as is clear from the discussion above, smaller pixels result in a weaker performance of the imager. It is a real challenge to improve pixel design and processing technology simultaneously so as to counteract the loss of performance due to shrinking pixels.

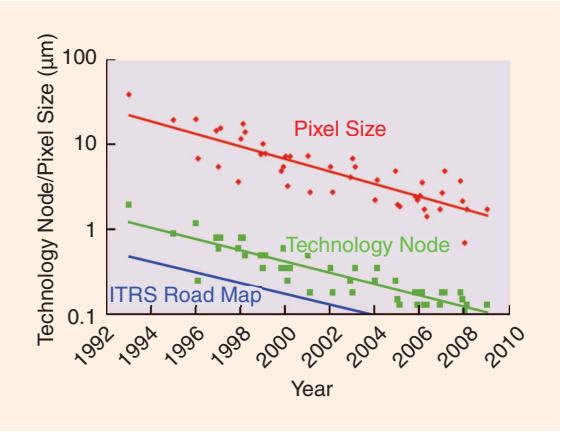

FIGURE 1: Evolution of the pixel size, the CMOS technology node used to fabricate the devices, and the minimum dimension according to the International Technology Roadmap for Semiconductors (ITRS).

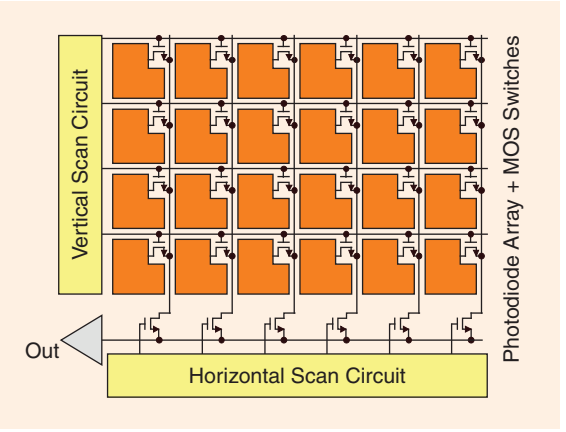

FIGURE 2: Architecture of a two-dimensional CMOS image sensor.

CMOS Pixel Architectures

In principle, the architecture of a CMOS image sensor is very similar to that of a digital memory (see Figure 2).

It is composed of:

- an array of identical pixels, each having at least a photodiode and an addressing transistor (the number of pixels today ranges from 330,000 for VGA-size imagers to 24 million or more for professional applications)
- a Y-addressing or scan register to address the sensor line-by-line, by activating the in-pixel addressing transistor
- an X-addressing or scan register to address the pixels on one line, one after another
- an output amplifier.

Figure 3 shows a photograph of an ultra-large area device intended for digital X-ray mammography.

The structure of the pixels can be very simple: a combination of a photodiode and an addressing transistor that acts as a switch (see Figure 4).

The working principle can be understood as follows [4]:

- At the beginning of an exposure, the photodiode is reverse-biased to a high voltage (e.g., 3.3 V).
- During the exposure time, impinging photons decrease the reverse voltage across the photodiode.
- At the end of the exposure time, the remaining voltage across the diode is measured; its drop from the original value is a measure for the amount of photons falling on the photodiode during the exposure time.
- To allow for a new exposure cycle, the photodiode is reset.

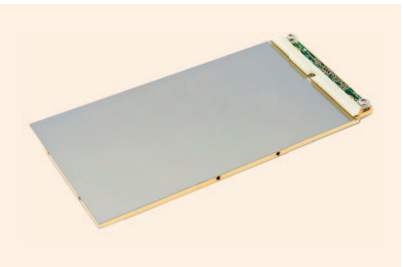

FIGURE 3: Photograph of a commercially available CMOS image sensor intended for X-ray mammography applications. Device area: 77 mm by 145 mm; pixel size: 33.55 μm by 33.55 μm; in total, 2,304 by 4,320 pixels. The design and packaging of this sensor is done in such a way that the packaged sensor is three-sided buttable. (Courtesy of DALSA Professional Imaging.)

This so-called passive pixel is characterized by a large fill factor (ratio of diode area and total pixel area), but unfortunately the pixel suffers from a large noise level as well. The reason for this is the mismatch between the small pixel capacitance and the large vertical bus capacitance.

CMOS image sensors have made significant technological progress over the last decade.

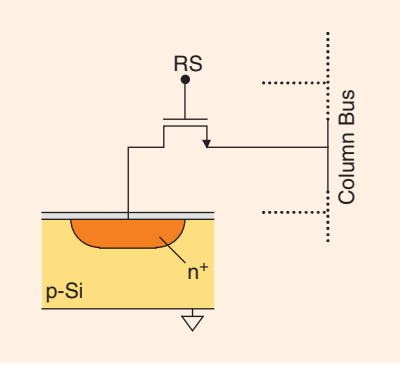

FIGURE 4: Passive CMOS pixel based on one in-pixel transistor, RS, used as the row-selection switch.

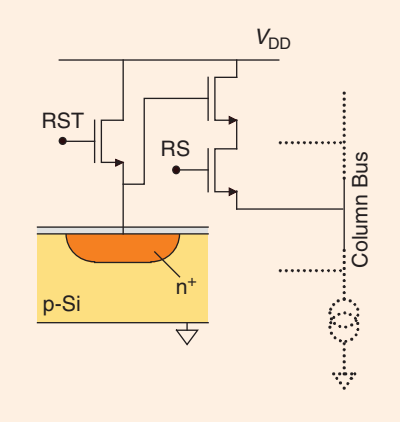

FIGURE 5: Active CMOS pixel based on an in-pixel amplifier. The transistors RST and RS are used for the resetting and selection of the pixel.

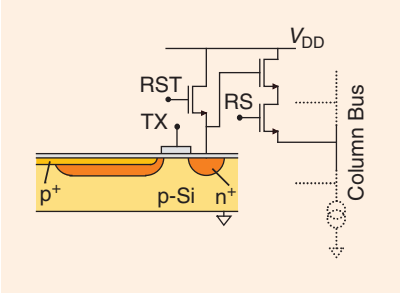

FIGURE 6: PPD CMOS pixel based on an in-pixel amplifier in combination with a PPD. RST, RS, and TX are respectively the reset, row select, and transfer transistors.

A major improvement in the noise performance of pixels was obtained by the introduction of the active pixel concept [5]–[7]. In this approach, every pixel gets its own in-pixel amplifier, being a source follower (see Figure 5).

The pixel is composed of the photodiode, the reset transistor, the driver of the source follower, and the addressing transistor. The current source of the source follower is placed at the end of the column bus. The working principle of the active pixel sensor (APS) is basically the same as for the passive pixel sensor:

- The photodiode is reverse-biased or reset.
- Impinging photons decrease the reverse voltage across the photodiode.
- At the end of the exposure time, the pixel is addressed and the voltage across the diode is brought outside the pixel by means of the source follower.
- The photodiode is reset again.

This concept of the APS became very popular in the mid-1990s because it solved a lot of noise issues. Unfortunately, the thermal kTC noise component, introduced by the resetting of the photodiode, remained.

To solve the issue of kTC FET noise in the presence of a filtering capacitor, the so-called pinned photodiode (PPD) pixel, also popular in CCD image sensors, was introduced. The PPD pixel has the great advantage of allowing correlated double sampling (CDS) to cancel the kTC noise of the reset action, the 1/f noise of the source follower MOS transistor, and the dc offset introduced by the source follower [8]. CDS in CMOS image sensors was demonstrated for the first time with a photogate APS pixel [9]. As was the case with CCDs, having the CDS option in CMOS imagers was a real breakthrough that allowed CMOS imagers to achieve higher performance.

The PPD APS, shown in Figure 6, can be seen as a logical improvement of the photogate APS since it combines the low noise performance achieved by means of CDS with the high light sensitivity and low dark current of a photodiode [10], [11].

At the right side of Figure 6, one can recognize exactly the same structure as in the APS. An extra (pinned) photodiode is added to this pixel, which is connected to the readout circuit by means of an extra transfer gate, TX. In this pixel, the photodiode is separated from the readout node. The PPD pixel operates as follows:

- Conversion of the incoming photons is performed in the PPD.
- At the end of the exposure, the readout node is reset by the reset transistor.
- A first measurement is done of the output voltage after reset.
- The photodiode is emptied by activating TX and transferring all charges from the photodiode to the readout node.
- A second measurement is made of the output voltage after transfer.
- The two measurements are subtracted from each other (this is the CDS step) [8].

The completely depleted PPD has several very attractive features:

- The kTC noise of the readout node can be completely cancelled by means of CDS.
- CDS also has a positive effect on the 1/f noise of the source follower, as well as on its residual offset.
- The kTC noise of the photodiode itself is completely absent because in case of full depletion, the photodiode can be made completely empty.

- The light sensitivity depends on the width of the depletion layer and consequently will be higher compared with a classical photodiode because the depletion layer of a PPD stretches almost to the Si-SiO_2 interface.
- Because of the double junction (p^+n and n-p substrate), the intrinsic charge storage capacitance is higher, resulting in a larger dynamic range.
- The Si-SiO_2 interface is perfectly shielded by the p^+ layer and keeps the interface fully filled with holes, which makes the leakage, or dark current, extremely low.

Considering all these advantages, it will be clear that the PPD is the preferred choice for CMOS image sensor pixels. Almost all products on the market these days make use of this pixel architecture, and it is the PPD that really boosted the introduction of CMOS image sensors into commercial products. Apparently history is repeating itself, since the CCD business also really took off after the introduction of the PPD [12].

The active CMOS pixel with a PPD is characterized by four transistors and five interconnections in each pixel, and this "complicated" architecture results in a relatively low fill factor. From the overview sketched in Figure 1, it is clear that it is very hard to make pixels smaller than 2.5 μm based on the PPD concept. The in-pixel periphery consumes too much space.

An answer to this issue can be found in the "shared pixel" concept: several neighboring pixels share the same output circuitry [13], [14]. The basic idea is illustrated in Figure 7.

A 2-by-2 pixel group has in common the source follower, the reset transistor, the addressing transistor, and the readout node. Aside from these components, the cluster of pixels has four PPDs and four transfer gates. The pixel timing becomes a bit more complicated, but the shared-pixel architecture is now characterized by eight interconnects and seven transistors, resulting in two interconnects and 1.75 transistors per photodiode.

The positive effect on the fill factor should be clear. The price one has to pay for the shared-pixel concept is an asymmetry in pixel design. The four individual PPDs of a cluster like that shown in Figure 7 are no longer perfectly identical to each other: within a square area, four PPDs and three transistors need to be placed. This results in a fixed-pattern noise component that needs to be corrected during the image-processing phase.

It is common knowledge that scaling effects in CMOS technology allow the semiconductor industry to make smaller devices.

Recently reported image sensors with pixel sizes smaller than 3 μm and even down to 1.15 μm are all based on the shared-pixel concept with PPDs [13].

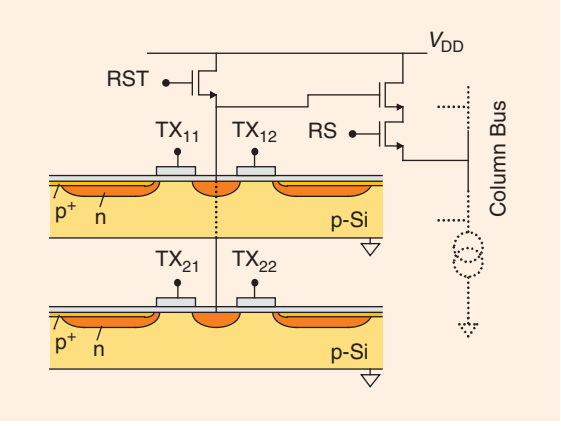

FIGURE 7: Shared-pixel concept: A 2-by-2 group of PPDs that share the same in-pixel readout circuitry. RST and RS are the reset and row select transistors, respectively; further selection of the individual pixels is accomplished by means of the various transfer (TX) gates.

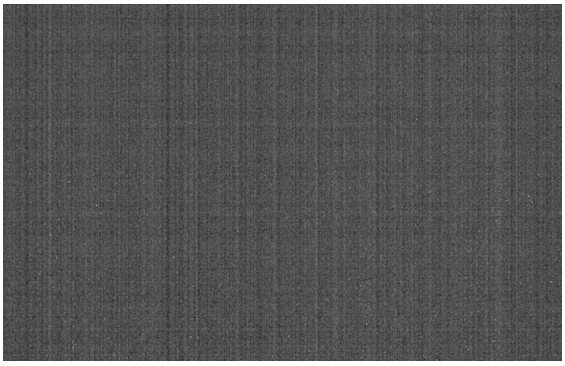

FIGURE 8: This image was produced by a test device made at Delft University of Technology. Clearly visible is the column-level fixed pattern noise. In this case, the column electronic circuitry is not properly biased. (Courtesy of Delft University of Technology.)

Photon Shot Noise

Image sensors are characterized by many different noise sources, which can be categorized into two groups: sources of temporal noise and sources of spatial noise. Examples are the following:

- **Temporal noise:** kTC noise, Johnson noise, flicker (1/f) noise, random telegraph signal (RTS) noise, dark-current shot noise, photon shot noise, power supply noise, phase noise, quantization noise.
- **Spatial noise:** dark fixed pattern, light fixed pattern, column fixed pattern, row fixed pattern, defect pixels, dead and sick pixels, scratches.

An example of fixed-pattern noise is shown in Figure 8: a combination of pixel FPN, row FPN, and column FPN dominates the performance of the sensor in dark.

Since it is not the purpose of this article to study all these sources of noise, only one important noise component will be discussed: photon shot noise. This is the noise component due to the statistical variation in the amount of photons impinging the sensor during the exposure time. This is a

stochastic process that can be described by Poisson statistics. If a pixel receives an amount of photons, equal to μ_{ph} during the exposure time, then this value μ_{ph} is the average value, which is also characterized by a noise component σ_{ph}, representing the photon shot noise. The relationship between the average value μ_{ph} and its associated noise σ_{ph} is given by:

$$\sigma_{ph} = \sqrt{\mu_{ph}}.$$

After absorption of the incoming photons into the silicon, the flux of μ_{ph} photons results in μ_e electrons in every pixel, characterized by a noise component σ_e and connected by the same square-root relation.

This ever-present photon shot noise component has a very interesting impact on the signal-to-noise behavior of an imaging system: in the case of a perfectly noise-free imager in a perfectly noise-free camera, the performance of the camera system is fully photon-shot-noise-limited. The maximum signal-to-noise ratio $(S/N)_{MAX}$ is then given by:

$$\left(\frac{S}{N}\right)_{MAX} = \frac{\mu_e}{\sigma_e} = \frac{\mu_e}{\sqrt{\mu_e}} = \sqrt{\mu_e},$$

or the maximum signal-to-noise ratio is equal to the square root of the signal value! This observation leads to an interesting rule of thumb: to make decent images for consumer applications, a minimum signal-to-noise ratio of 40 dB or more is needed, which translates by means of the above-mentioned formula into 10,000 electrons within every pixel. This number tends to go down slowly with extensive image processing and image-noise removal.

As CMOS technology continues to shrink, allowing for smaller pixels, the lower limit of pixel size will no longer be determined by the minimum dimensions set by the CMOS technology but by the number of electrons that can be stored in each pixel.

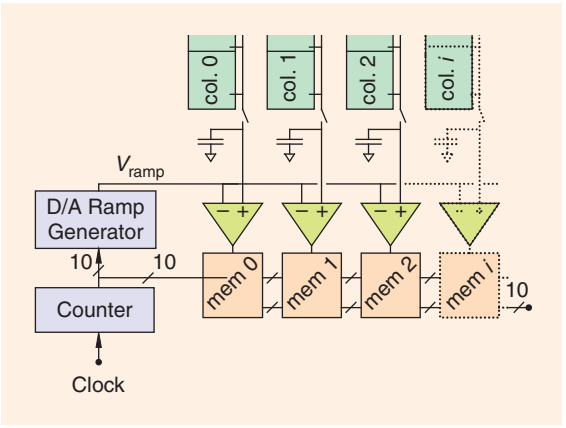

FIGURE 9: Basic architecture of a column-parallel single-slope ADC.

Analog-to-Digital Converters for CMOS Image Sensors

It should be clear that in the era of digital imaging, most CMOS image sensors are provided with an analog-to-digital converter (ADC) allowing the output signal to be accessible in the digital domain. Classical ADC architectures can be used in combination with the CMOS imager, e.g., flash converter, sigma-delta converter, successive approximation, single-slope ADC, pipelined ADC, cyclic ADC, and so forth. Only one architecture will be discussed in this article: the single-slope ADC. This concept is very appealing when the CMOS imager is provided with an ADC for every column or even for every pixel. In particular, column-parallel conversion has some very interesting advantages for high-speed applications, because in this case the sensor chip has as many ADCs as it has columns and all these ADCs work fully in parallel [15]–[17].

The basic working principle of the single-slope ADC is illustrated in Figure 9.

The analog input signal V_{IN} that needs to be converted is compared with an analog ramp signal V_{ramp}. A digital counter generates the latter. At the moment that the two voltages V_{IN} and V_{ramp} are equal to each other, the comparator changes state and latches the counter value into a memory. The data stored into the memory will be the digital value corresponding to the analog input voltage V_{IN}. In the case of column-parallel conversion, the imager has a comparator and a digital memory for every column. The digital counter is common for all pixels on a single row.

After digitization, the output signal of the camera will have an extra quantization noise component σ_{ADC} that can be described by:

$$\sigma_{ADC} = \frac{V_{LSB}}{\sqrt{12}},$$

where V_{LSB} is the analog voltage of the least significant bit.

In relation to photon shot noise, an interesting observation

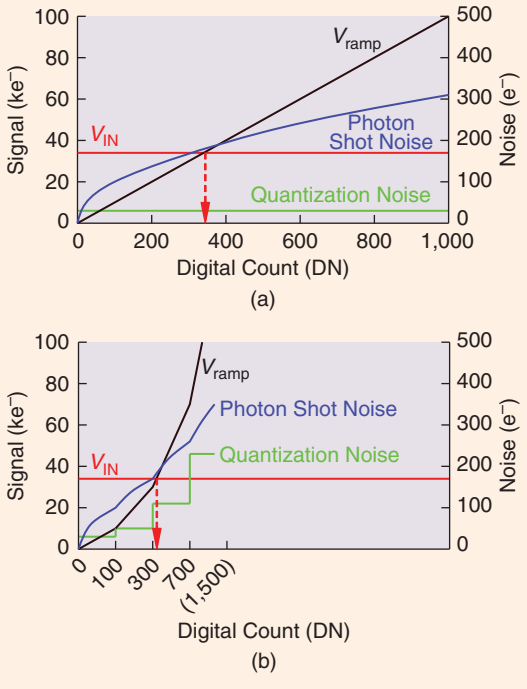

FIGURE 10: Ramp voltage for (a) the single slope and (b) the multislope ADC, in relation to the photon shot noise and quantization noise.

can be made: the noise floor in the output signal of an image sensor is best case determined by the photon shot noise. The latter will be small for small output signals of the sensor but large for large output signals of the sensor. In the case of a large output signal, the quantization error of the ADC does not have to be as low as it should be for smaller output signals. This idea allows an ADC converter with an adaptive quantization step: small for small signals, large for large signals. Such a scheme can be relatively easily implemented by means of the single-slope ADC. In this case the ramp, generated originally by the digital counter, will no longer be linear with respect to time but will make use of a piecewise-linear approach, as shown in Figure 10 [18].

In Figure 10, next to the ramp itself the photon shot noise is indicated as well as the quantization noise. It can be seen that when the quantization step is increased, the quantization noise is increased as well. But as long as it stays well below the photon shot noise, it will not hamper the performance of the sensor. In this simple example (in which the quantization noise is kept a factor of two below the photon shot noise), the ADC is changing from a single-slope to a so-called multislope ADC. In this way, its speed is increased by a factor of three without further increasing its power consumption.

Another way to increase the speed of the single-slope ADC is by using a single-slope, multiple-ramp concept. In this configuration, several ramps run in parallel. They all have the same slope, but they differ from each other by a dc offset [19]. Before starting the conversion, a coarse ADC action is performed to assign every column of the image sensor to a dedicated ramp. The coarse conversion is followed by a fine

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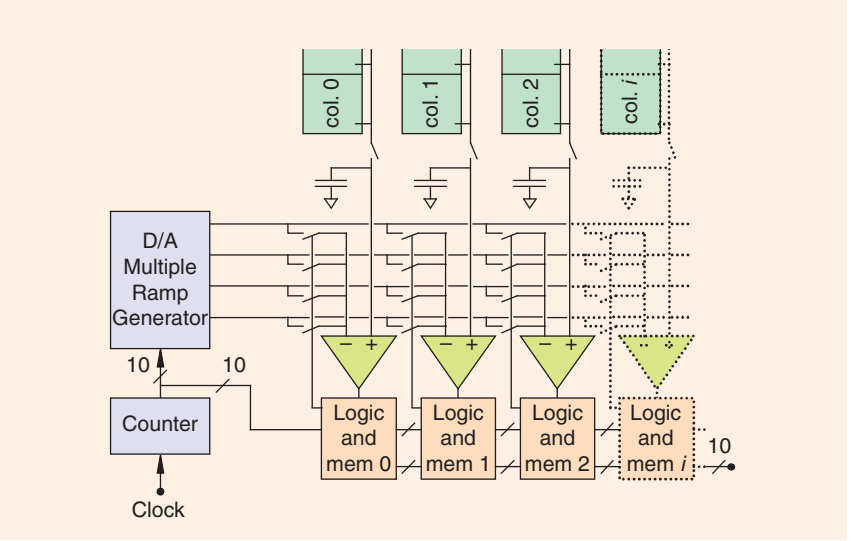

FIGURE 11: Basic architecture of a column-parallel, single-slope, multiramp ADC.

conversion cycle, and at the end both results are combined. In Figure 11, the multiple-ramp concept is illustrated: at first the coarse action takes place, and its output is memorized in a two-bit memory cell (two bits in this example, with four parallel ramps).

These two bits not only represent the most significant bits of the digital words but also contain the information as to which ramp the column needs to be assigned to for the fine conversion. During the latter, the four parallel ramps are offered to all columns, but every column is checked against only one particular ramp. It should be clear that the increase in speed is approximately equal to the number of parallel ramps (disregarding the time needed to perform the coarse ADC). Figure 12 shows a chip photograph of a CMOS image sensor provided with a multislope, multiramp column-level ADC.

This example of implementing a single-slope, multiple-ramp, column-parallel ADC architecture demonstrates a key advantage of

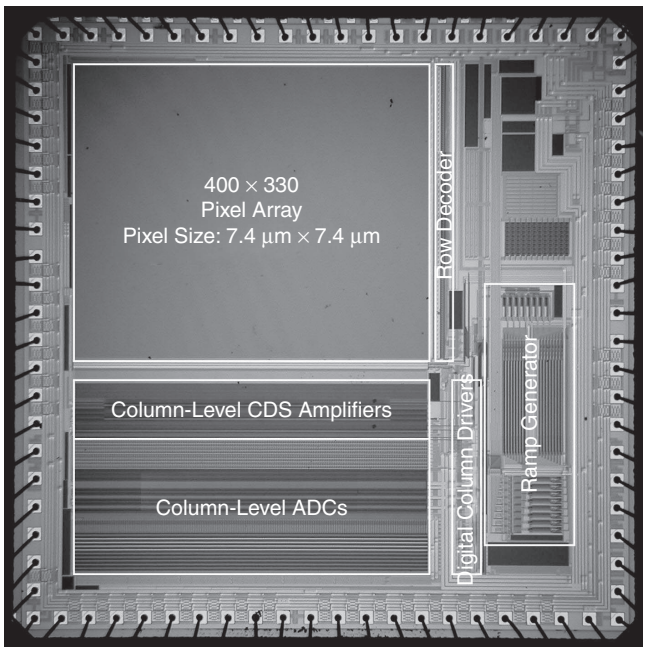

FIGURE 12: Microphotograph of a test chip designed in one of the Delft University of Technology Ph.D. projects. The intention of this device was to prove the concept of the multislope, multiramp, column-level ADC. (Courtesy of Delft University of Technology.)

CMOS image sensors: one can implement additional analog and digital circuitry on the same chip as the imaging core. In the meantime, the noise characteristics of the imager are taken into account when seeking to improve this on-chip circuitry as far as speed and power consumption are concerned.

Conclusions

CMOS image sensors have made significant technological progress over the last decade. The introduction of the pinned photodiode greatly boosted their success. Exploring the typical characteristics, needs, and requirements of imaging applications can result in very attractive circuits and devices that increase the performance of the imagers. Because of the ever-shrinking dimensions of CMOS technology, further integration at the column level and even the pixel level can make the imagers even smarter than they already are.

Acknowledgments

The author would like to thank all the imaging-community colleagues who contributed to the R&D of solid-state image sensors. Special thanks go to the people who did a lot of pioneering work on CMOS imagers in the early 1990s. They not only introduced new technical, market, and business opportunities but also challenged CCDs to increase their price-performance ratios as never before.

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About the Author

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